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DEVELOPMENTS IN HIGH RESOLUTION TDI CMOS IMAGING FOR SPACE APPLICATIONS

Abstract

The highly integrated nature of CMOS processing allows for a significant reduction in auxiliary drive equipment compared with equivalent CCD imaging technology. On-chip ADCs and clock generation, coupled with multiple arrays on a single chip render CMOS imaging devices highly suitable for small satellite applications with high spectral versatility where cost and payload weight can be substantial feasibility drivers.

Recognizing the opportunity for a Small Satellite offering in the very high resolution market, Surrey Satellite Technology Ltd (SSTL) have been working in partnership with Te2v to integrate state of the art sensors into the 'Precision' payload. Through innovative manufacturing techniques, and a novel sensor architecture, Precision will have a market leading performance for its size, weight and power.

The CIS125 is a 16k pixel width detector with four panchromatic and six multispectral arrays of 5m and 10m pitch respectively. Designed features include PAN channel half pixel offset for super-resolution and charge transfer bi-directionality for focal plane integration. The in-parallel readout nature afforded by CMOS technology allows for peak signal to be measured at high line rates – key drivers towards improved ground resolution. Payload power consumption is also reduced from CCD counterparts through the integration of drivers onto the chip itself allowing for smaller, more affordable focal planes.

This paper will provide an overview of the Precision payload specification and design as well as the innovative aspects of the Precision sensor, including their current status and qualification work completed. Results from characterised detectors demonstrating TDI performance outputs as well as digital capability from the CIS125 will be presented with parameters such as charge transfer limited full well capacity and noise being discussed in the frame of achievable signal to noise ratios. Planned future developments for the sensor (including anticipated QE and MTF performance), supporting equipment and payload roadmaps as TRL drivers will be discussed.