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THE SOFTWARE ARCHITECTURE OF PROXIMITY SPACE COMMUNICATION FOR SMALL MARS MISSION

Abstract

Currently, there is an increasing interest for many countries to launch probers to Mars. Because of the really long distance between earth and Mars, the optimization of the mass and power consumption and the enhancement of reliability become extraordinary critical especially for small satellites. The CCSDS proximity-1 protocol gives three communication modes for Mars probes (such as orbiter and rover) in proximity space, which are full duplex mode, half duplex mode and simplex mode. Considering the requirements of deep space exploration mission for product miniaturization and low power consumption, the rover and orbiter generally only support 1-2 working modes. For example, Odyssey MER CE-505 UHF transceiver only supports full duplex mode. Furthermore, more deep space missions only support simplex mode. Therefore, if the three communication modes could be fused without increasing resources, additional chips and power consumption, the proximity space communication in deep space exploration mission will be more flexible and reliable. In this paper, the software architecture of proximity space communication for small Mars mission is presented. In this method, the screaming processing part and the specific functional part in full duplex mode, half duplex mode and simplex mode are separated from the main frame, and the fusing design is carried out to form a general VHDL (Very-High-Speed Integrated Circuit Hardware Description Language) structure, and the other scheduling control parts are integrated into the soft core of the FPGA. Besides, only limited FPGA resource is used to implement proximity-1 protocol instead of FPGA and DSP, which is protected by TMR (triple modular redundancy) and timing scrub to decrease the SEE influence. The method is also carried in Chinese first Mars exploration mission (TW-1). By using the conception product which embeds 1 Altera Stratix III FPGA, real test result shows that the presented method performs well and the needed FPGA resource only are 45% slice, 51% DSP and 38% RAM.