IAF SPACE SYSTEMS SYMPOSIUM (D1)
Space Systems Architectures (2)

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A HIGH-PERFORMANCE MASS MEMORY UNIT FOR NEXT GENERATION SATELLITE SYSTEMS

Abstract

In modern satellite systems, the mass memory unit (MMU) is a key element for storing and retrieving payload data generated on the satellite itself. In many satellite applications, however, the data rate and data volume of the payload (e.g. scientific instruments) significantly exceeds the capacity of the downlink channel. Here, we present the current status of a high-performance but reliable MMU development for next generation satellite systems, that will be able to reach data rates up to 20 GBit with a storage capacity of more than 40 TBit. To this end, the actual architectural design implementation details as well as the future roadmap are shown.

The MMU architecture can be roughly split up into two separate domains for input/output monitoring (IOM) and the mass memory module (MMM). The IOM part exploits a Microsemi RTG4 FPGA, for the handling of high-speed interfaces for data acquisition from the instrumentation and data playback to the downlink transceiver. In general, various State-of-the-Art (SotA) interconnects can be considered, such as WizardLink, SpaceWire or SpaceFibre. The IOM design is flexible and the actual interfaces can be adapted to the specific mission requirements. Moreover, the IOM also manages the data routing between the external interfaces and the MMM part.

The MMM part bases on the radiation-tolerant Xilinx XQRKU060 Ultrascale FPGA that controls a DDR3 8GByte working memory for buffering the incoming and outgoing data. Besides its extremely high computational performance, it also provides the ability to perform firmware updates (partial reconfiguration) at runtime in space. The interconnection between IOM and MMM is established by 12 HSSL lines operating at 2 GBit/s each.

Both IOM and MMM parts are accompanied by a hard-wired controller that is used to run the boot loader and application software of the MMU that is responsible for application software updates and the overall orchestration of the data flow, respectively.

Besides the processing elements, the memory storage device itself is also a key element of the proposed MMU architecture. Because of its high density, the use of NAND Flash components for space-grade MMUs

has become established in recent years. However, for the targeted storage capacity, the capability of existing space-grade Flashes are insufficient. Hence, a comprehensive up-screening of suitable commercial Flash devices has to be taken into account, which will be able to satisfy the high technical requirements and, at the same time, increases the competitiveness of the MMU as a product.