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Author: Dr. Rafal Graczyk
University of Luxembourg, Luxembourg , rafal.graczyk@uni.lu

Mr. Saad Memon
University of Luxembourg, Luxembourg , saad.memon@uni.lu
Prof. Marcus Völp
University of Luxembourg, Luxembourg , marcus.voelp@uni.lu

METHODS FOR INCREASING THE DEPENDABILITY OF HIGH PERFORMANCE, MANY-CORE, SYSTEM-ON-CHIPS

Abstract

Future of space exploration and exploitation will require significantly increased autonomy of system operation, for mission planning, decision making and adaptive control techniques, new processing and compression algorithms, and, very often augmented with Machine Learning and Artificial Intelligence capabilities. This potential will have to be provided with robustness, reliability and dependability levels sufficient for conducting successful mission. In building equipment for space, one has to trade system robustness for the high processing capabilities and low energy consumption. The high performance, low robustness approach, is acceptable, especially in Earths' vicinity, when assets are protected by the planet's magnetosphere. However, in more demanding environments, in cis-lunar or deep space, high energy particles will affect the modern components heavily, causing temporary or permanent damage, and affecting the systems' dependability. State-of-the-art processing elements (processors, co-processors, memories and, all integrates, System-on-Chips, or, SoCs) are superior to their high reliability, space qualified, counterparts in terms of processing power or in terms of electrical power supply. For processing performance, 2-3 orders of magnitude more performance, per electric power unit is expected from modern, stat-of-the-art devices. On the other hand, the gap of at least 9 technology nodes (between high reliability and high performance devices) leads to 25 times decrease of power consumption per operation. The enormous improvements of performance in modern semiconductor devices bears promise, that some of this excess processing power can be utilized, in building a combination of hardware and software mechanisms that is capable of increasing robustness and resilience of otherwise susceptible semiconductor devices, while allowing to harness the remaining processing power to build affordable space systems with large degrees of autonomy, rich functionality and high bandwidth. We're bridging this performance-reliability gap, by researching the enabling building blocks for constructing more reliable and more secure System-on-Chips. We address this problem, by introducing trusted, small cross-section subcomponents of System-On-Chip, that equip the operating system with what is needed to fight radiation-induced faults (latch-ups) in a flexible and adaptable manner. We introduce the hardware and software controlled rejuvenation (core refresh) mechanism) of a processor core that grants flexibility to adjust fault masking robustness in relation to the current radiation level the system is exposed to.